

T1440-VB TO251 Datasheet

N-Channel 650V (D-S) Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	650	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	4
Q_g (Max.) (nC)	11	
Q_{gs} (nC)	2.3	
Q_{gd} (nC)	5.2	
Configuration	Single	

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC


RoHS
 COMPLIANT


ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	650	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current ^e	V _{GS} at 10 V	T _C = 25 °C	I _D	2.0	A
Continuous Drain Current		T _C = 100 °C		1.28	
Pulsed Drain Current ^a			I _{DM}	8	
Linear Derating Factor				0.48	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	165	mJ
Repetitive Avalanche Current ^a			I _{AR}	2	A
Repetitive Avalanche Energy ^a			E _{AR}	6	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	45	W
Peak Diode Recovery dV/dt ^c			dV/dt	2.8	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 24\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 3.2\text{ A}$ (see fig. 12).
- $I_{SD} \leq 3.2\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- Drain current limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.1	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		650	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^d		-	670	-	mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1 A ^b	-	4.0	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1 A		3.9	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	417	-	pF
Output Capacitance	C _{oss}			-	45	-	
Reverse Transfer Capacitance	C _{rss}			-	5	-	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	912	-	
			V _{DS} = 520 V, f = 1.0 MHz	-	26		
Effective Output Capacitance	C _{oss eff.}	V _{DS} = 0 V to 520 V ^c		-	42	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 12 A, V _{DS} = 400 V see fig. 6 and 13 ^b	-	-	11	nC
Gate-Source Charge	Q _{gs}			-	-	2.3	
Gate-Drain Charge	Q _{gd}			-	-	5.2	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 325 V, I _D = 1.2A R _G = 9.1 Ω, R _D = 62 Ω, see fig. 10 ^b		-	14	-	ns
Rise Time	t _r			-	20	-	
Turn-Off Delay Time	t _{d(off)}			-	34	-	
Fall Time	t _f			-	18	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	8	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 3.2 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 3.2 A, dI/dt = 100 A/μs ^b		-	180	230	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	2.1	3.2	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
 c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
 d. $t = 60\text{ s}$, $f = 60\text{ Hz}$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

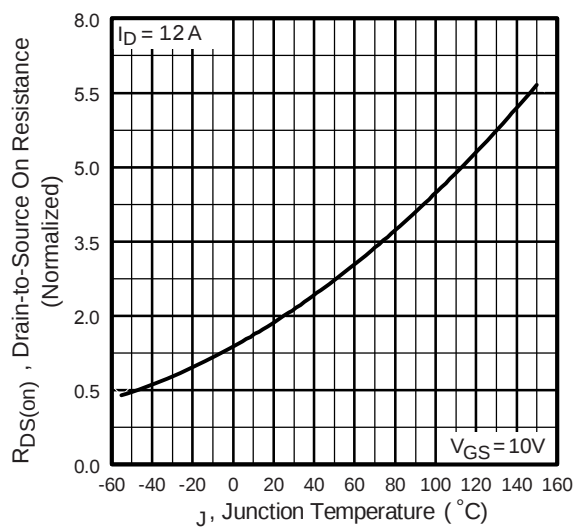
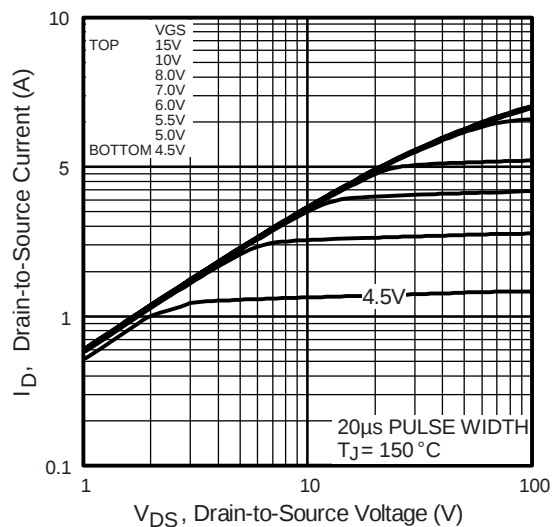
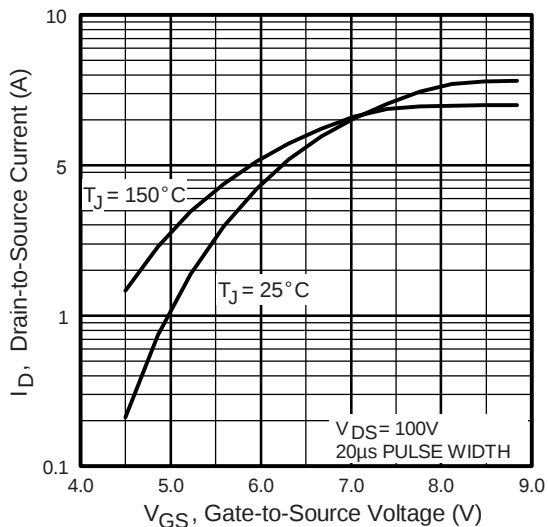
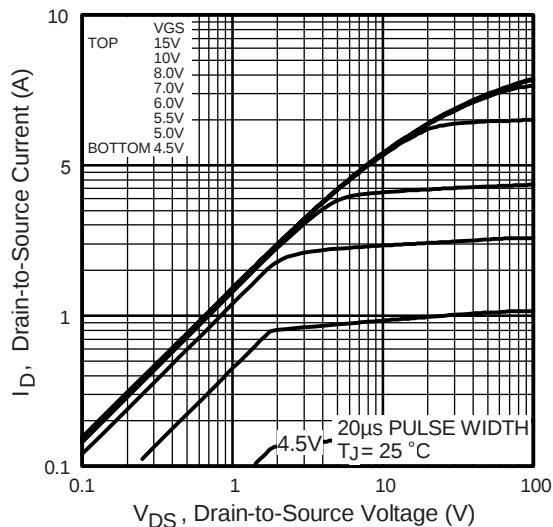




Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Maximum Drain Current vs. Case Temperature

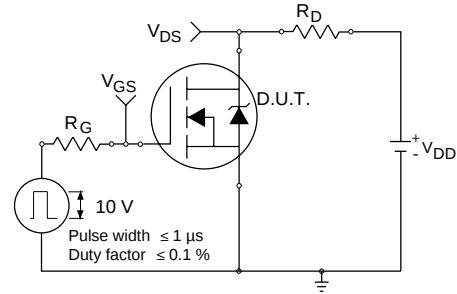


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit

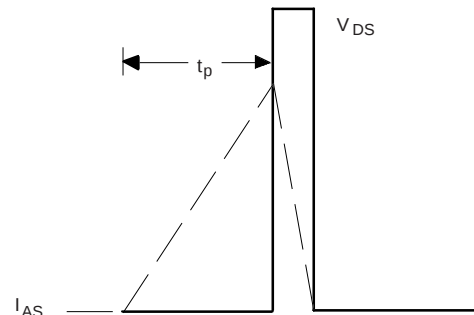


Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current

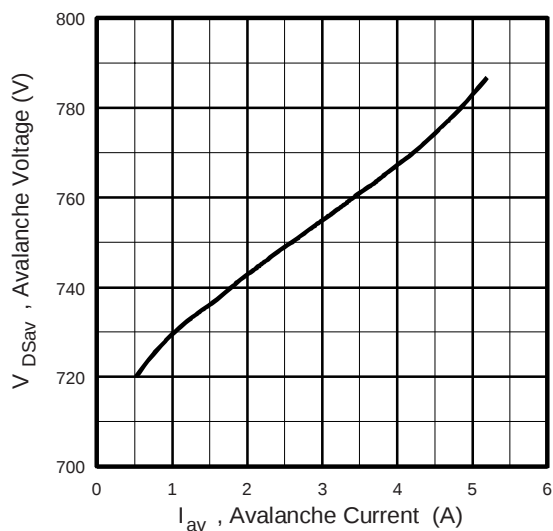


Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current

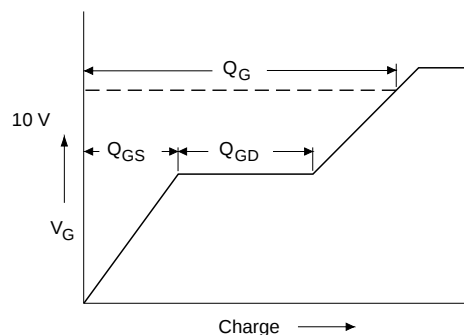


Fig. 13a - Basic Gate Charge Waveform

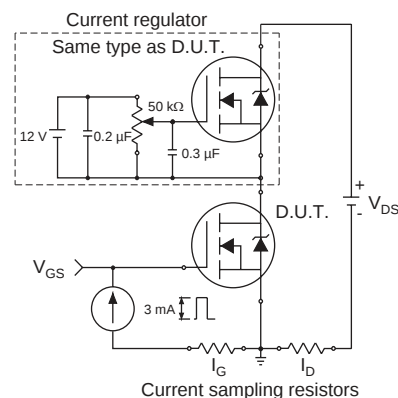


Fig. 13b - Gate Charge Test Circuit

The diagram illustrates a switching circuit for a Device Under Test (D.U.T.). The circuit includes a MOSFET driver stage (labeled ②) with a transformer-coupled gate driver, a MOSFET (labeled ③), and a load inductor (labeled ④). The D.U.T. is represented by a MOSFET symbol (labeled ①) connected to the gate of the MOSFET (labeled ③). The gate of the MOSFET (labeled ③) is connected to the primary of the transformer (labeled ②). The secondary of the transformer is connected to the gate of the MOSFET (labeled ③). The drain of the MOSFET (labeled ③) is connected to a load inductor (labeled ④) and a MOSFET (labeled ①). The MOSFET (labeled ①) is connected to the gate of the MOSFET (labeled ③). The MOSFET (labeled ③) is connected to the drain of the MOSFET (labeled ①). The MOSFET (labeled ③) is connected to the drain of the MOSFET (labeled ①). The MOSFET (labeled ③) is connected to the drain of the MOSFET (labeled ①).

Circuit layout considerations

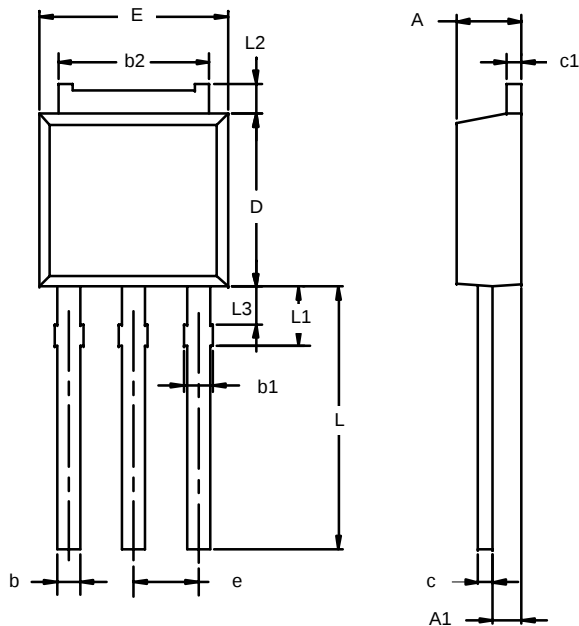
- Low stray inductance
- Ground plane
- Low leakage inductance current transformer

Device Under Test (D.U.T.)

- dV/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by duty factor "D"
- D.U.T. - device under test



TO-251AA



Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
b	0.71	0.89	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.43	0.206	0.214
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
E	6.48	6.73	0.255	0.265
e	2.28 BSC		0.090 BSC	
L	3.89	9.53	0.153	0.375
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060

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